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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,870	08/27/2001	Yoko Hayashida	N26180400W	4837

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Darryl G. Walker
WALKER & SAKO, LLP
Suite 235
300 South First Street
San Jose, CA 95113

EXAMINER
NGUYEN, DANNY

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,870	HAYASHIDA ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's arguments see page number 6 filed 01/08/2003, with respect to the rejection(s)of claim(s) 3, 4, 9,12, 16-18 under APA have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of APA and Kouno.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Kouno (USPN 6,385,028). APA discloses that a method for designing a semiconductor integrated circuit device including IGFET (see fig. 17) comprises executing a simulation with a predetermined charged device model (CDM) circuit that includes a first clamping device (111a) connected to an I/O terminal (110a), a first IGFET (112a) having a gate connected to the I/O terminal through a first resistance (R114a), a second clamping device (113b) connected between gate and source/drain terminals of the first IGFET and connected to a supply potential wiring (117), the first and second clamping devices being connected to one another through a second resistance (wiring resistance 117). APA does not disclose the step of selecting a ratio of the second resistance and the first resistance as claimed. Kouno discloses selecting a ratio of the second resistance (wiring resistance Rg) and the first resistance

(the input impedance Z of the transistor 52, see col. 8, lines 28-60). It would have been obvious to one having ordinary skill in the art of the time the invention was made to modify the circuit of APA with a ratio resistance as taught by Kouno in order to prevent surge voltage applied to drain terminal of the transistor.

3. Claims 1-3, 7, 8, 10-13, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Taillient (USPN 5,515,226).

Regarding to claims 1, 3,15, APA discloses that an apparatus for a semiconductor integrated circuit device (see fig. 17) comprises a plurality of transistors (112a to 112c) coupled to a corresponding I/O terminal (110a to 110c) through a corresponding first resistance (R114a to R114c); a first clamping device (111a) coupled to each I/O terminal (110a); a second clamping circuit (113a to 113c) corresponding to each transistor, each second clamping circuit including a second clamping device (113a) and the corresponding the first resistance, each second clamping device having a first terminal connected to the gate of the corresponding transistor (112a to 112c) and a second terminal connected to a source/drain of the corresponding transistor and a supply potential wiring (117); each first clamping device being coupled to one second clamping device through a second resistance (wiring resistance 117). APA does not disclose that at least two of the second clamping devices are different. Taillient discloses that a second limiter (EC2j) of semiconductor integrated circuit device (fig. 4C) can be varied depending on the location of the transistor. Taillient discloses the second limiter (EC2j) of transistor (ELj) can be varied depending on the protection level needed by he transistor (ELj) due to its location relative to the pad which it is connected to (see

col. 3, lines 15-19). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to utilize the teaching of Taillient in order to vary the second clamping circuit of APA in order to provide the protection as needed by the individual transistor depending on its location and protected level needed.

Regarding to claim 2, APA discloses that a supply potential wiring is selected from the group of consisting of an electric power supply potential wiring (118), and a ground electric potential wiring, and a substrate electric potential wiring (117) (see p. 3, lines 2-3).

4. Claims 5 and 6, the APA in view of Taillient disclose all limitations of claim 1. APA and Taillient do not disclose that a length of wiring connects the second clamping devices (113a) to the gate and the drain/source of the corresponding transistor (112a) is no more than 100 micrometers. However, It would have been obvious to one having ordinary skill in the art at the time invention was made to substitute a length of wiring to any desired values as long as it compatible with the requirements of the other components in the integrated circuit in order to minimize any resistance between its components. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding to claim 7, APA discloses that the first resistance (R114) comprises a wiring resistance and contact resistance (see fig. 15).

Regarding to claim 8, APA discloses that the first resistance includes a non-wiring structure (internal resistor 114a.

Regarding to claim 10, APA discloses that the second resistance (114a) comprises a supply potential wiring (118) and a contact resistance where the first and second clamping devices are connected to the supply potential wiring (118) (see fig. 18).

Regarding to claim 11, APA discloses that the semiconductor integrated circuit device (see fig. 18) comprises each first clamping device (111a) has a first terminal connected to one of the I/O terminal (110a), a second terminals of each first clamping device being connected to the second terminal (110b) of one of the second clamping device (111b) by system wiring (118) of at least one supply terminal; and the second resistance (114a) comprises a contact resistance between the second terminal of the first clamping device and the supply potential wiring, a contact resistance between the second terminal of the second clamping device (113a).

Regarding to claims 12 and 13, APA does not disclose that each first clamping device (111a) and each second clamping device connected to a different supply terminal. Taillient discloses the first clamping circuit (EC1j) and second clamping circuit (EC2j) are connected to different power supply terminal (between Pj and P1, see fig. 3). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to utilize the teaching of Taillient in order to vary the second clamping circuit of APA in order to provide the protection as needed by the individual transistor depending on its location and protected level needed.

5. Claim 14, APA in view of Taillient disclose all limitations of claim 1 except for each second clamping device selected from a group as claimed. As for the clamping

device being various elements (an IGFET, an NPN bipolar, a diode, and a thyristor); it would have been obvious to one of ordinary skill in the art at the time the invention was made to select any known over-voltage protection element as deemed suitable in order to provide the over-voltage protection function. This is further demonstrated by applicant's various embodiments of the over-voltage protection as claimed absent persuasive evidence that particular type of over-voltage protection element is significant.

6. Claim 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Taillient et al., and further in view of Matshara et al. (USPN 5,942,916). APA and Taillient disclose all limitations except for having an effective channel resistance. Matshara et al. disclose having an effective channel resistance (fig. 16A). Therefore, it would have been obvious to one having ordinary skill in the art at the time invention was made to modify the circuit of APA and Taillient with an effective channel resistance as taught by Matshara et al. in order to provide a wide range resistance to be selected (Matshara et al., col. 9, lines 55-59).

Response to Arguments

7. Applicant's arguments filed 01/08/2003 which are based on claims 1, 3, 15 have been fully considered but they are not persuasive.

Regarding to claim 1, the applicant argued that there is no teaching or suggesting at least two of the second clamping circuits that vary from one another in the Tailliet reference. However, Taillient does teach that dimensions of the second clamping circuits (EC2j) will vary, depending on the values of the input resistor Rj (see col. 4,

lines 43-47). In addition, the resistance of ground bus (BM) can vary according to the position of the input/output terminals (Pj). Therefore, the variation of the (EC2j) arises due to the differences of the wiring resistance of ground bus (BM) and the input terminal resistor (Rj). Thus, the applicant's claim 1 does not distinguish over Taillient reference. Dependent claims 3 and 15 are also rejected at least by virtue of their dependency on independent claim 1.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-305-1341 for regular communications and (703)-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

DN

D.N.
March 7, 2003

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800